### SPECIAL FEATURES
- 4096 bits of Read/Write Nonvolatile Memory
- 256-bit Scratchpad Ensures Integrity of Data Transfer
- Memory Partitioned into 256-bit Pages for Packetizing Data
- Data Integrity Assured with Strict Read/Write Protocols
- Contains Real-Time Clock/Calendar in Binary Format
- Interval Timer Can Automatically Accumulate Time When Power is Applied
- Programmable Cycle Counter can Accumulate the Number of System Power-On/Off Cycles
- Programmable Alarms Can Be Set to Generate Interrupts for Interval Timer, Real-Time Clock, and/or Cycle Counter
- Write-Protect Feature Provides Tamperproof Time Data
- Programmable Expiration Date That Limits Access to SRAM and Timekeeping
- Clock Accuracy is Better Than ±2 Minutes/Month at 25°C
- Operating Temperature Range from -40°C to +70°C
- Over 10 Years of Data Retention

### COMMON iButton FEATURES
- Unique, Factory-Lasered, and Tested 64-bit Registration Number (8-bit Family Code + 48-bit Serial Number + 8-bit CRC Tester) Assures Absolute Traceability Because No Two Parts Are Alike
- Multidrop Controller for 1-Wire Network
- Digital Identification and Information by Momentary Contact
- Chip-Based Data Carrier Compactly Stores Information
- Data Can Be Accessed While Affixed to Object
- Economically Communicates to Bus Master with a Single Digital Signal at 16.3kbps
- Standard 16mm Diameter and 1-Wire® Protocol Ensure Compatibility with iButton Family
- Button Shape is Self-Aligning with Cup-Shaped Probes
- Durable Stainless Steel Case Engraved with Registration Number Withstands Harsh Environments
- Easily Affixed with Self-Stick Adhesive Backing, Latched by its Flange, or Locked with a Ring Pressed onto its Rim
- Presence Detector Acknowledges when Reader First Applies Voltage
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for Use in Class I, Division 1, Group A, B, C and D Locations

### ORDERING INFORMATION
DS1994L-F5+   F5 MicroCan
+Denotes a lead(Pb)-free/RoHS-compliant package.

### EXAMPLES OF ACCESSORIES
- DS9096P Self-Stick Adhesive Pad
- DS9101 Multi-Purpose Clip
- DS9093RA Mounting Lock Ring
- DS9093F Snap-In Fob
- DS9092 iButton Probe

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**iButton DESCRIPTION**

The DS1994 Memory iButton is a rugged read/write data carrier that acts as a localized database, easily accessible with minimal hardware. The nonvolatile memory and optional timekeeping capability offer a simple solution to storing and retrieving vital information pertaining to the object to which the iButton is attached. Data is transferred serially through the 1-Wire protocol that requires only a single data lead and a ground return.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory. A 48-bit serial number is factory lasered into each DS1994 to provide a guaranteed unique identity that allows for absolute traceability. The durable MicroCan package is highly resistant to environmental hazards such as dirt, moisture, and shock. Its compact, coin-shaped profile is self-aligning with mating receptacles, allowing the DS1994 to be easily used by human operators. Accessories permit the DS1994 to be mounted on almost any surface including plastic key fobs, photo-ID badges, and PC boards.

The DS1994 also includes time-keeping functions, a real-time clock/calendar, interval timer, cycle counter, and programmable interrupts, in addition to the nonvolatile memory. The internal clock can be programmed to deny memory access based on absolute time/date, total elapsed time, or the number of accesses. These features allow the DS1994 to be used to create a stopwatch, alarm clock, time and date stamp, logbook, hour meter, calendar, system power cycle timer, interval timer, and event scheduler.

**OPERATION**

The DS1994 has four main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 4096-bit SRAM, and 4) timekeeping registers. The timekeeping section utilizes an on-chip oscillator that is connected to a 32.768kHz crystal. The SRAM and time-keeping registers reside in one contiguous address space referred to hereafter as memory. All data is read and written least significant bit first.

The memory functions are not available until the ROM function protocol has been established. This protocol is described in the ROM functions flowchart (Figure 9). The master must first provide one of four ROM function commands: 1) read ROM, 2) match ROM, 3) search ROM, or 4) skip ROM. After a ROM function sequence has been successfully executed, the memory functions are accessible and the master can then provide any one of the four memory function commands (Figure 6).
PARASITE POWER
The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry steals power whenever the data input is high. The data line provides sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is not consumed for 1-Wire ROM function commands, and 2) if the battery is exhausted for any reason, the ROM may still be read normally. The remaining circuitry of the DS1994 is solely operated by battery energy.

64-BIT LASERED ROM
Each DS1994 contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. (See Figure 2.) The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates, as shown in Figure 3. The polynomial is $X^8 + X^3 + X^4 + 1$. Additional information about the 1-Wire Cyclic Redundancy Check is available in Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products. The shift register bits are initialized to zero. Then starting with the least significant bit of the family code, 1 bit at a time is shifted in. After the 8th bit of the family code has been entered, then the serial number is entered. After the 48th bit of the serial number has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC should return the shift register to all zeros.

Figure 2. 64-BIT LASERED ROM

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
<th>MSB</th>
<th>LSB</th>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Bit CRC Code</td>
<td>48-Bit Serial Number</td>
<td>8-Bit Family Code (04h)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 3. 1-WIRE CRC CODE

```
Polynomial = x^8 + x^5 + x^4 + 1
```

**MEMORY**

The memory map in Figure 4 shows a 32-Byte page called the scratchpad, and additional 32-Byte pages called memory. The DS1994 contains 16 pages that make up the 4096-bit SRAM. The DS1994 also contains page 16, which has only 30 Bytes containing the timekeeping registers.

The scratchpad is an additional page that acts as a buffer when writing to memory. Data is first written to the scratchpad where it can be read back. After the data has been verified, a copy scratchpad command transfers the data to memory. This process ensures data integrity when modifying the memory.

**TIMEKEEPING**

A 32.768kHz crystal oscillator is used as the time base for the timekeeping functions. The oscillator can be turned on or off by an enable bit in the control register. The oscillator must be on for the real-time clock, interval timer, and cycle counter to function.

The timekeeping functions are double buffered. This feature allows the master to read time or count without the data changing while it is being read. To accomplish this, a snapshot of the counter data is transferred to holding registers that the user accesses. This occurs after the 8th bit of the read memory function command.

**Real-Time Clock**

The real-time clock is a 5-Byte binary counter. It is incremented 256 times per second. The least significant Byte is a count of fractional seconds. The upper 4 Bytes are a count of seconds. The real-time clock can accumulate 136 years of seconds before rolling over. Time/date is represented by the number of seconds since a reference point, which is determined by the user. For example, 12:00 A.M., January 1, 1970 could be a reference point.
Figure 4. DS1994 MEMORY MAP

NOTE: Each page is 32 bytes (256 bits). The hex values represent the starting address for each page or register.

PAGE 0
- 0000h
- 0020h
- 0040h
- 0060h
- 0080h

PAGE 1
- 00A0h

PAGE 2
- 00C0h

PAGE 3
- 00E0h

PAGE 4
- 0100h

PAGE 5
- 0120h

PAGE 6
- 0140h

PAGE 7
- 0160h

PAGE 8
- 0180h

PAGE 9
- 01A0h

PAGE 10
- 01C0h

PAGE 11
- 01E0h

PAGE 12

PAGE 13

PAGE 14

PAGE 15

PAGE 16
- 0200h

PAGE 16
- STATUS REGISTER
- CONTROL REGISTER
- REAL-TIME COUNTER REGISTERS
- INTERVAL TIME COUNTER REGISTERS
- CYCLE COUNTER REGISTERS
- REAL-TIME ALARM REGISTERS
- INTERVAL TIME ALARM REGISTERS
- CYCLE ALARM REGISTERS

STATUS REGISTER

CONTROL REGISTER

DSEL STOP AUTO MAN OSC RO WPC WPI WPR

STOP START AUTOMAN

0200h

0201h
Interval Timer
The interval timer is a 5-Byte binary counter. When enabled, it is incremented 256 times per second. The least significant Byte is a count of fractional seconds. The interval timer can accumulate 136 years of seconds before rolling over. The interval timer has two modes of operation that are selected by the AUTO/MAN bit in the control register. In the auto mode, the interval timer begins counting after the data line has been high for a period of time determined by the DSEL bit in the control register. Similarly, the interval timer stops counting after the data line has been low for a period of time determined by the DSEL bit. In the manual mode, time accumulation is controlled by the STOP/START bit in the control register.

NOTE: For auto mode operation, the high level on the data line must be greater than or equal to 2.1V.

Cycle Counter
The cycle counter is a 4-Byte binary counter. It increments after the falling edge of the data line if the appropriate data line timing has been met. This timing is selected by the DSEL bit in the control register. (See the Status/Control section).

NOTE: For cycle counter operation, the high level on the data line must be greater than or equal to 2.1V.

Alarm Registers
The alarm registers for the real-time clock, interval timer, and cycle counter all operate in the same manner. When the value of a given counter equals the value in its associated alarm register, the appropriate flag bit is set in the status register. If the corresponding interrupt enable bit in the status register is set, an interrupt is generated. If a counter and its associated alarm register are write protected when an alarm occurs, access to the device becomes limited. (See the Status/Control, Interrupts, and Programmable Expiration sections.)

STATUS/CONTROL REGISTERS
The status and control registers are the first two Bytes of page 16 (see Figure 4).

Status Register

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>CCE</td>
<td>ITE</td>
<td>RTE</td>
<td>CCF</td>
<td>ITF</td>
<td>RTF</td>
</tr>
</tbody>
</table>

0200h

DON’T CARE BITS

READ ONLY

0 RTF Real-time clock alarm flag
1 ITF Interval timer alarm flag
2 CCF Cycle counter alarm flag
When a given alarm occurs, the corresponding alarm flag is set to a logic 1. The alarm flag is cleared by reading the status register.

3 **RTE** Real-time clock alarm flag
4 **ITE** Interval timer alarm flag
5 **CCE** Cycle counter alarm flag

Writing any of the interrupt enable bits to a logic 0 allows an interrupt condition to be generated when its corresponding alarm flag is set (see the *Interrupts* section).

### Control Register

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DSEL</strong></td>
<td>STOP</td>
<td>START</td>
<td><strong>AUTO</strong></td>
<td><strong>MAN.</strong></td>
<td><strong>OSC</strong></td>
<td><strong>RO</strong></td>
<td><strong>WPC</strong></td>
</tr>
<tr>
<td>0</td>
<td>WPR</td>
<td>Write protect real-time clock/alarms registers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>WPI</td>
<td>Write protect interval timer/alarms registers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>WPC</td>
<td>Write protect cycle counter/alarms registers</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Setting a write protect bit to a logic 1 permanently write protects the corresponding counter and alarm registers, all write protect bits, and additional bits in the control register. The write protect bits cannot be written in a normal manner (see the *Write Protect/Programmable Expiration* section).

3 **RO** Read only

If a programmable expiration occurs and the read only bit is set to a logic 1, then the DS1994 becomes read only. If a programmable expiration occurs and the read only bit is a logic 0, then only the 64-bit lasered ROM can be accessed (see the *Write Protect/Programmable Expiration* section).

4 **OSC** Oscillator enable

This bit controls the crystal oscillator. When set to a logic 1, the oscillator starts operation. When the oscillator bit is a logic 0, the oscillator stops.

5 **AUTO/MAN** Automatic/Manual Mode

When this bit is set to a logic 1, the interval timer is in automatic mode. In this mode, the interval timer is enabled by the data line. When this bit is set to a logic 0, the interval timer is in manual mode. In this mode, the interval timer is enabled by the STOP/START bit.
6 **STOP/START** Stop/Start (in manual mode)

If the interval timer is in manual mode, the interval timer starts counting when this bit is set to a logic 0 and stops counting when set to a logic 1. If the interval timer is in automatic mode, this bit has no effect.

7 **DSEL** Delay Select Bit

This bit selects the delay that it takes for the cycle counter and the interval timer (in auto mode) to see a transition on the data line. When this bit is set to a logic 1, the delay time is $123 \pm 2\text{ms}$. This delay allows communication on the data line without starting or stopping the interval timer and without incrementing the cycle counter. When this bit is set to a logic 0, the delay time is $3.5 \pm 0.5\text{ms}$.

**MEMORY FUNCTION COMMANDS**

The Memory Function Flowchart (Figure 6) describes the protocols necessary for accessing the memory. An example follows the flowchart. Three address registers are provided as shown in Figure 5. The first two registers represent a 16-bit target address (TA1, TA2). The third register is the ending offset/data status Byte (E/S).

The target address points to a unique Byte location in memory. The first 5 bits of the target address (T4:T0) represent the Byte offset within a page. This Byte offset points to one of 32 possible Byte locations within a given page. For instance, `00000b` points to the first Byte of a page whereas `11111b` would point to the last Byte of a page.

The third register (E/S) is a read only register. The first 5 bits (E4:E0) of this register are called the ending offset. The ending offset is a Byte offset within a page (1 of 32 Bytes). Bit 5 (PF) is the partial Byte flag. Bit 6 (OF) is the overflow flag. Bit 7 (AA) is the authorization accepted flag.

**Figure 5. ADDRESS REGISTERS**

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>T7</td>
<td>T6</td>
<td>T5</td>
<td>T4</td>
<td>T3</td>
<td>T2</td>
<td>T1</td>
<td>T0</td>
</tr>
<tr>
<td>T15</td>
<td>T14</td>
<td>T13</td>
<td>T12</td>
<td>T11</td>
<td>T10</td>
<td>T9</td>
<td>T8</td>
</tr>
<tr>
<td>AA</td>
<td>OF</td>
<td>PF</td>
<td>E4</td>
<td>E3</td>
<td>E2</td>
<td>E1</td>
<td>E0</td>
</tr>
</tbody>
</table>
Write Scratchpad Command [0Fh]
After issuing the write scratchpad command, the user must first provide the 2-Byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the Byte offset (T4:T0). The ending offset (E4:E0) is the Byte offset at which the host stops writing data. The maximum ending offset is 11111b (31d). If the host attempts to write data past this maximum offset, the overflow flag (OF) is set and the remaining data is ignored. If the user writes an incomplete Byte and an overflow has not occurred, the partial Byte flag (PF) is set.

Read Scratchpad Command [AAh]
This command can be used to verify scratchpad data and target address. After issuing the read scratchpad command, the user can begin reading. The first two Bytes are the target address. The next Byte is the ending offset/data status Byte (E/S), followed by the scratchpad data beginning at the Byte offset (T4:T0). The user can read data until the end of the scratchpad, after which the data read is all logic 1’s.

Copy Scratchpad [55h]
This command is used to copy data from the scratchpad to memory. After issuing the copy scratchpad command, the user must provide a 3-Byte authorization pattern. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). If the pattern matches, the AA (authorization accepted) flag is set and the copy begins. A logic 0 is transmitted after the data has been copied until the user issues a reset pulse. Any attempt to reset the part is ignored while the copy is in progress. Copy typically takes 30μs.

The data to be copied is determined by the three address registers. The scratchpad data, from the beginning offset through the ending offset, is copied to memory, starting at the target address. Anywhere from 1 to 32 Bytes can be copied to memory with this command. Whole Bytes are copied even if only partially written. The AA flag is cleared only by executing a write scratchpad command.

Read Memory [F0h]
The read memory command can be used to read the entire memory. After issuing the command, the user must provide the 2-Byte target address. After the two Bytes, the user reads data beginning from the target address and can continue until the end of memory, at which point logic 1’s are read. It is important to realize that the target address registers contain the address provided. The ending offset/data status Byte is unaffected.

The hardware of the DS1994 provides a means to accomplish error-free writing to the memory section. To safeguard reading data in the 1-Wire environment and to simultaneously speed up data transfers, it is recommended to packetize data into data packets of the size of one memory page each. Such a packet would typically store a 16-bit CRC with each page of data to ensure rapid, error-free data transfers that eliminate having to read a page multiple times to determine if the received data is correct or not. (Refer to Application Note 114 for the recommended file structure to be used with the 1-Wire environment.)
Figure 6. MEMORY FUNCTIONS FLOWCHART

Master TX Memory Function Command

0FH Write Scratchpad

To Figure 6
Second Part

Y

Bus Master TX TA1 (T7:T0)

Bus Master TX TA2 (T15:T8)

Bus Master RX TA1 (T7:T0)

Bus Master RX TA2 (T15:T8)

DS1994 sets Scratchpad Offset = (T4:T0) and Clears (PF, OF, AA)

DS1994 sets (E4:E0) = Scratchpad Offset

Master TX Data Byte To Scratchpad Offset

DS1994 sets (E4:E0) = Scratchpad Offset

Bus Master TX Reset?

Scratchpad Offset = 11111b?

Partial Byte Written?

Bus Master TX Data?

OF = 1

Bus Master TX Reset?

Y

Y

Y

N

N

N

N

Y

N

N

Partial Byte Written?

PF = 1

Bus Master RX *1’s

From Figure 6
Second Part

Partial Byte Written?

DS1994 Increments Scratchpad Offset

Y

N

From Figure 6
Second Part

DS1994 TX Presence Pulse (See Figure 9)
Figure 6. MEMORY FUNCTIONS FLOWCHART (continued)

From Figure 6
First Part

Scratchpad

Copy

55H

N

Y

Bus Master TX
TA1 (T7:T0)

Bus Master TX
TA2 (T15:T8)

Bus Master TX
E/S Byte

Auth.
Code Match

N

Y

AA = 1

DS1994 TX "1"s

DS1994 Copies
Scratchpad Data
To Memory

DS1994 TX "0"s

Bus Master TX
TA1 (T7:T0)

Bus Master TX
TA2 (T15:T8)

Bus Master TX
TA1 (T7:T0)

Bus Master TX
TA2 (T15:T8)

DS1994 sets Memory
Address = (T15:T0)

Master RX Data
Byte From
Memory Address

DS1994

Increments
Address Counter

Y

Bus Master
TX Reset

Y

Bus Master
TX Reset

N

N

Bus Master
TX Reset

Bus Master
TX Reset

N

Memory
Address = 21Dh

Y

Bus Master RX "1"s

To Figure 6
First Part
MEMORY FUNCTION EXAMPLES
Example: Write two data Bytes to memory locations 0026h and 0027h (the seventh and eighth Bytes of page 1). Read entire memory.

<table>
<thead>
<tr>
<th>MASTER MODE</th>
<th>DATA (LSB FIRST)</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>Reset</td>
<td>Reset pulse (480μs–960μs)</td>
</tr>
<tr>
<td>RX</td>
<td>Presence</td>
<td>Presence pulse</td>
</tr>
<tr>
<td>TX</td>
<td>CCh</td>
<td>Issue skip ROM command</td>
</tr>
<tr>
<td>TX</td>
<td>0Fh</td>
<td>Issue write scratchpad command</td>
</tr>
<tr>
<td>TX</td>
<td>26h</td>
<td>TA1, beginning offset = 6</td>
</tr>
<tr>
<td>TX</td>
<td>00h</td>
<td>TA2, address = 0026h</td>
</tr>
<tr>
<td>TX</td>
<td>&lt;2 data Bytes&gt;</td>
<td>Write 2 Bytes of data to scratchpad</td>
</tr>
<tr>
<td>TX</td>
<td>Reset</td>
<td>Reset pulse</td>
</tr>
<tr>
<td>RX</td>
<td>Presence</td>
<td>Presence pulse</td>
</tr>
<tr>
<td>TX</td>
<td>CCh</td>
<td>Issue skip ROM command</td>
</tr>
<tr>
<td>TX</td>
<td>AAh</td>
<td>Issue read scratchpad command</td>
</tr>
<tr>
<td>RX</td>
<td>26h</td>
<td>Read TA1, beginning offset = 6</td>
</tr>
<tr>
<td>RX</td>
<td>00h</td>
<td>Read TA2, address = 0026h</td>
</tr>
<tr>
<td>RX</td>
<td>07h</td>
<td>Read E/S, ending offset = 7, flags = 0</td>
</tr>
<tr>
<td>RX</td>
<td>&lt;2 data Bytes&gt;</td>
<td>Read scratchpad data and verify</td>
</tr>
<tr>
<td>TX</td>
<td>Reset</td>
<td>Reset pulse</td>
</tr>
<tr>
<td>RX</td>
<td>Presence</td>
<td>Presence pulse</td>
</tr>
<tr>
<td>TX</td>
<td>CCh</td>
<td>Issue skip ROM command</td>
</tr>
<tr>
<td>TX</td>
<td>55h</td>
<td>Issue copy scratchpad command</td>
</tr>
<tr>
<td>TX</td>
<td>26h</td>
<td>TA1</td>
</tr>
<tr>
<td>TX</td>
<td>00h</td>
<td>TA2 AUTHORIZATION CODE</td>
</tr>
<tr>
<td>TX</td>
<td>07h</td>
<td>E/S</td>
</tr>
<tr>
<td>TX</td>
<td>Reset</td>
<td>Reset pulse</td>
</tr>
<tr>
<td>RX</td>
<td>Presence</td>
<td>Presence pulse</td>
</tr>
<tr>
<td>TX</td>
<td>CCh</td>
<td>Issue skip ROM command</td>
</tr>
<tr>
<td>TX</td>
<td>F0h</td>
<td>Issue read memory command</td>
</tr>
<tr>
<td>TX</td>
<td>00h</td>
<td>TA1, beginning offset = 6</td>
</tr>
<tr>
<td>TX</td>
<td>00h</td>
<td>TA2, address = 0000h</td>
</tr>
<tr>
<td>RX</td>
<td>&lt;542 Bytes&gt;</td>
<td>Read entire memory</td>
</tr>
<tr>
<td>TX</td>
<td>Reset</td>
<td>Reset pulse</td>
</tr>
<tr>
<td>RX</td>
<td>Presence</td>
<td>Presence pulse, done</td>
</tr>
</tbody>
</table>
WRITE PROTECT/PROGRAMMABLE EXPIRATION

The write protect bits (WPR, WPI, WPC) provide a means of write protecting the timekeeping data and limiting access to the DS1994 when an alarm occurs (programmable expiration). The write protect bits cannot be written by performing a single copy scratchpad command. Instead, to write these bits, the copy scratchpad command must be performed three times. Please note that the AA bit is set, as expected, after the first copy command is successfully executed. Therefore, the authorization pattern for the second and third copy command should have this bit set. The read scratchpad command can be used to verify the authorization pattern.

The write protect bits, once set, permanently write protect their corresponding counter and alarm registers, all write protect bits, and certain control register bits as shown in Figure 7. The time/count registers continue to count if the oscillator is enabled. If the user wishes to set more than one write protect bit, the user must set them at the same time. Once a write protect bit is set it cannot be undone, and the remaining write protect bits, if not set, cannot be set. The programmable expiration takes place when one or more write protect bits have been set and a corresponding alarm occurs. If the RO (read only) bit is set, only the read scratch and read memory function commands are available. If the RO bit is a logic 0, no memory function commands are available. The ROM functions are always available.

Figure 7. WRITE PROTECT CHART

<table>
<thead>
<tr>
<th>WRITE PROTECT BIT SET:</th>
<th>WPR</th>
<th>WPI</th>
<th>WPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Protected from User Modification:</td>
<td>Real-Time Clock</td>
<td>Interval Timer</td>
<td>Cycle Counter</td>
</tr>
<tr>
<td></td>
<td>Real-Time Alarm</td>
<td>Interval Time Alarm</td>
<td>Cycle Counter Alarm</td>
</tr>
<tr>
<td></td>
<td>WPR</td>
<td>WPI</td>
<td>WPC</td>
</tr>
<tr>
<td></td>
<td>RO</td>
<td>OSC*</td>
<td>STOP/START **</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>AUTO/MAN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Becomes write 1 only, i.e., once written to a logic 1, cannot be written back to a logic 0.
** Forced to a logic 0.

1-WIRE BUS SYSTEM

The 1-Wire bus is a system that has a single bus master and one or more slaves. In most instances, the DS1994 behaves as a slave. The exception is when the DS1994 generates an interrupt due to a timekeeping alarm. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS1994 is open drain with an internal circuit equivalent to that shown in Figure 8. A multidrop bus consists of a 1-Wire bus with multiple slaves attached. The 1-Wire bus has a maximum data rate of 16.3kbps and requires a pullup resistor of approximately 5kΩ. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 120μs, one or more of the devices on the bus can be reset.
TRANSACTION SEQUENCE
The protocol for accessing the DS1994 through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory Function Command
- Transaction/Data

INITIALIZATION
All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master, followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1994 is on the bus and is ready to operate. For more details, see the 1-Wire Signaling section.

ROM FUNCTION COMMANDS
Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (see the flowchart in Figure 9).

Read ROM [33h]
This command allows the bus master to read the DS1994’s 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single DS1994 on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48–bit serial number usually result in a mismatch of the CRC.

Match ROM [55h]
The match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1994 on a multidrop bus. Only the DS1994 that exactly matches the 64-bit ROM sequence responds to the subsequent memory function command. All slaves that do not match the 64-bit ROM sequence wait for a reset pulse. This command can be used with a single or multiple devices on the bus.
Figure 9. ROM FUNCTIONS FLOWCHART
Skip ROM [CCh]
This command can save time in a single drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Search ROM [F0h]
When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their 64-bit ROM codes. The search ROM command allows the bus master to use a process of elimination to identify the 64-bit ROM codes of all slave devices on the bus. The search ROM process is the repetition of a simple three–step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple, three-step routine on each bit of the ROM. After one complete pass, the bus master knows the contents of the ROM in one device. Additional passes can identify the remaining number of devices and their ROM codes. Refer to Application Note 187: 1-Wire Search Algorithm for a detailed discussion, including an example.

Search Interrupt [ECh]
This ROM command works exactly as the normal ROM Search, but it identifies only devices with interrupts that have not yet been acknowledged.

1-WIRE SIGNALING
The DS1994 requires strict protocols to ensure data integrity. The protocol consists of five types of signaling on one line: reset sequence with reset pulse and presence pulse, write 0, write 1, read data, and interrupt pulse. The bus master initiates all these signals except presence pulse and interrupt pulse. The initialization sequence required to begin any communication with the DS1994 is shown in Figure 10. A reset pulse followed by a presence pulse indicates the DS1994 is ready to send or receive data given the correct ROM command and memory function command. The bus master transmits (Tx) a reset pulse ($t_{RSTL}$, minimum 480$\mu$s). The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus is pulled to a high state through the pullup resistor. After detecting the rising edge on the data line, the DS1994 waits ($t_{PDH}$, 15$\mu$s to 60$\mu$s) and then transmits the presence pulse ($t_{PDL}$, 60$\mu$s to 240$\mu$s). There are special conditions if interrupts are enabled for which the bus master must check the state of the 1-Wire bus after being in the Rx mode for 480$\mu$s. These conditions are discussed in the Interrupt section.

READ/WRITE TIME SLOTS
The definitions of write and read time slots are illustrated in Figure 11. The master driving the data line low initiates all time slots. The falling edge of the data line synchronizes the DS1994 to the master by triggering a delay circuit in the DS1994. During write time slots, the delay circuit determines when the DS1994 samples the data line. For a read data time slot, if a 0 is to be transmitted, the delay circuit determines how long the DS1994 holds the data line low overriding the 1 generated by the master. If the data bit is a 1, the button leaves the read data time slot unchanged.
Figure 10. INITIALIZATION PROCEDURE RESET AND PRESENCE PULSES

![Diagram showing the INITIALIZATION PROCEDURE RESET AND PRESENCE PULSES](image)

- $V_{PULLUP}$
- $V_{PULLUP\ MIN}$
- $V_{IH\ MIN}$
- $V_{IL\ MAX}$
- $0\ V$

- $t_{RSTL}$
- $t_{R}$
- $t_{PDH}$
- $t_{PDL}$
- $t_{RSTH}$

- Master TX "RESET PULSE"
- Master RX "PRESENCE PULSE"

- RESISTOR
- MASTER
- DS1994

- $480\ \mu s \leq t_{RSTL} < \infty^*$
- $480\ \mu s \leq t_{RSTH} < \infty^{**}$
- $15\ \mu s \leq t_{PDH} < 60\ \mu s$
- $60 \leq t_{PDL} < 240\ \mu s$

* In order not to mask interrupt signaling by other devices on the 1-Wire bus, $t_{RSTL}$ + $t_{R}$ should always be less than 960 us.

** Includes recovery time

Figure 11. READ/WRITE TIMING DIAGRAM

Write-One Time Slot

![Diagram showing the WRITE-TIME TIMING DIAGRAM](image)

- $V_{PULLUP}$
- $V_{PULLUP\ MIN}$
- $V_{IH\ MIN}$
- $V_{IL\ MAX}$
- $0\ V$

- $t_{SLOT}$
- $t_{REC}$
- $t_{LOW1}$

- RESISTOR
- MASTER

- $60\ \mu s \leq t_{SLOT} < 120\ \mu s$
- $1\ \mu s \leq t_{LOW1} < 15\ \mu s$
- $1\ \mu s \leq t_{REC} < \infty$
Interrupts

If the DS1994 detects an alarm condition, it automatically sets the corresponding alarm flag in the status register. An interrupt condition begins whenever any alarm flag is set and the flag’s corresponding interrupt bit is enabled. The interrupt condition ceases when the alarm flags are cleared (i.e., the interrupt is acknowledged by reading the status register, address 200H) or if the corresponding interrupt enable bit is disabled.

The DS1994 can produce two types of interrupts: spontaneous interrupts, called type 1, and delayed interrupts, type 2. Spontaneous interrupts need to be armed by a reset pulse after all communication on the 1-Wire bus has finished. A single falling slope on the 1-Wire bus disarms this type of interrupt. If an alarm condition occurs while the device is disarmed, at first a type 2 interrupt is produced.
Spontaneous interrupts are signaled by the DS1994 by pulling the data line low for $960\mu$s to $3840\mu$s as the interrupt condition begins (Figure 12). After this long low pulse, a presence pulse follows. If the alarm condition occurs just after the master has sent a reset pulse, i.e., during the high or low time of the presence pulse, the DS1994 does not assert its interrupt pulse until the presence pulse is finished (Figure 13).

If the DS1994 cannot assert a spontaneous interrupt, either because the data line was not pulled high, communication was in progress, or the interrupt was not armed, it extends the next reset pulse to a total length of $960\mu$s to $3840\mu$s (delayed interrupt). If the alarm condition occurs during the reset low time of the reset pulse, the DS1994 immediately asserts its interrupt pulse; thus, the total low time of the pulse can be extended up to $4800\mu$s (Figure 14). If a DS1994 with a not previously signaled alarm detects a power-on cycle on the 1-Wire bus, it sends a presence pulse and waits for the reset pulse sent by the master to extend it and to subsequently issue a presence pulse (Figure 15). As long as an interrupt has not been acknowledged by the master, the DS1994 continues sending interrupt pulses.

The interrupt signaling discussed so far is valid for the first opportunity the device has to signal an interrupt. It is not required for the master to acknowledge an interrupt immediately. If an interrupt is not acknowledged, the DS1994 continues signaling the interrupt with every reset pulse. To do so, the DS1994 either uses the waveform of the type 2 interrupt (Figure 14) or the waveform of the type 1A interrupt (Figure 13). The waveform of the type 2 interrupt is observed after a communication to a device other than the interrupting one; after successful communication to the interrupting device (without acknowledging the interrupt), the waveform of the type 1A interrupt is found.

**Figure 12. TYPE 1 INTERRUPT**

![Figure 12. TYPE 1 INTERRUPT](image)
Figure 13. TYPE 1A INTERRUPT (SPECIAL CASE)

Interrupt condition occurs during the presence pulse, but the interrupt is not generated until the presence pulse is completed.

Figure 14. TYPE 2 INTERRUPT

Interrupt condition exists prior to master releasing reset.

Figure 15. TYPE 2 INTERRUPT (SPECIAL CASE)

Interrupt condition occurs while the bus is powered down. Bus powers up.

LINE TYPE LEGEND:
- Bus master active low
- Both bus master and DS1994 active low
- DS1994 active low
- Resistor pullup
PHYSICAL SPECIFICATIONS
Size See mechanical drawing
Weight 3.3 grams (F5 package)
Expected Service Life 10 years at 25°C
Safety Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, Approved under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations

ABSOLUTE MAXIMUM RATINGS*
Voltage on any Pin Relative to Ground -0.5V to +7.0V
Operating Temperature -40°C to +70°C
Storage Temperature -40°C to +70°C

* This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS (-40°C to +70°C)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-Wire Pullup Voltage</td>
<td>( V_{PUP} )</td>
<td>2.8</td>
<td></td>
<td>6.0</td>
<td>V</td>
<td>1, 2</td>
</tr>
<tr>
<td>Logic 1</td>
<td>( V_{IH} )</td>
<td>2.2</td>
<td></td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Logic 0</td>
<td>( V_{IL} )</td>
<td>-0.3</td>
<td></td>
<td>+0.8</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Output Logic Low at 4mA</td>
<td>( V_{OL} )</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Input Load Current</td>
<td>( I_{L} )</td>
<td></td>
<td>5</td>
<td></td>
<td>( \mu )A</td>
<td>3</td>
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CAPACITANCE (\( T_A = 25°C \))

<table>
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<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O (1-Wire)</td>
<td>( C_{IN/OUT} )</td>
<td>100</td>
<td>800</td>
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<td>pF</td>
<td>6, 8</td>
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AC ELECTRICAL CHARACTERISTICS (\( V_{PUP} = 2.8V \) to 6.0V; -40°C to +70°C)

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<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Slot</td>
<td>( t_{SLOT} )</td>
<td>60</td>
<td>120</td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>Write 1 Low Time</td>
<td>( t_{LOW1} )</td>
<td>1</td>
<td>15</td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>Write 0 Low Time</td>
<td>( t_{LOW0} )</td>
<td>60</td>
<td>120</td>
<td></td>
<td>( \mu )s</td>
<td></td>
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<tr>
<td>Read Data Valid</td>
<td>( t_{RDV} )</td>
<td>exactly 15</td>
<td></td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>Release Time</td>
<td>( t_{RELEASE} )</td>
<td>0</td>
<td>15</td>
<td>45</td>
<td>( \mu )s</td>
<td></td>
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<tr>
<td>Read Data Setup</td>
<td>( t_{SU} )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu )s</td>
<td>5</td>
</tr>
<tr>
<td>Interrupt</td>
<td>( t_{INT} )</td>
<td>960</td>
<td>4800</td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>Recovery Time</td>
<td>( t_{REC} )</td>
<td>1</td>
<td></td>
<td></td>
<td>( \mu )s</td>
<td></td>
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<tr>
<td>Reset Time High</td>
<td>( t_{RSTH} )</td>
<td>480</td>
<td></td>
<td></td>
<td>( \mu )s</td>
<td>4</td>
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<tr>
<td>Reset Time Low</td>
<td>( t_{RSTL} )</td>
<td>480</td>
<td>960</td>
<td></td>
<td>( \mu )s</td>
<td>7</td>
</tr>
<tr>
<td>Presence Detect High</td>
<td>( t_{PDH} )</td>
<td>15</td>
<td>60</td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
<tr>
<td>Presence Detect Low</td>
<td>( t_{PDL} )</td>
<td>60</td>
<td>240</td>
<td></td>
<td>( \mu )s</td>
<td></td>
</tr>
</tbody>
</table>
Note 1: All voltages are referenced to ground.

Note 2: $V_{PUP} =$ external pullup voltage, see Figure 8.

Note 3: Input load is to ground.

Note 4: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 5: Read data setup time refers to the time the host must pull the 1-Wire bus low to read a bit. Data is guaranteed to be valid within 1$\mu$s of this falling edge and remains valid for 14$\mu$s minimum. (15$\mu$s total from falling edge on 1-Wire bus.)

Note 6: Capacitance on the data line could be 800pF when power is first applied. If a 5k$\Omega$ resistor is used to pull up the data line to $V_{PUP}$, 5$\mu$s after power has been applied, the parasite capacitance does not affect normal communications.

Note 7: The reset low time ($t_{RSTL}$) should be restricted to a maximum of 960$\mu$s to allow interrupt signaling; otherwise, it could mask or conceal interrupt pulses.

Note 8: Guaranteed by design, not production tested.
REVISION HISTORY

<table>
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<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
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<td>7/08</td>
<td>Updated the F5 MicroCan face brand with the latest per PCN H020201.</td>
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<td>11/09</td>
<td>• Updated the ordering information to lead-free.</td>
<td>1, 3, 16, 21, 22</td>
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<td>• Replaced &quot;MicroLAN&quot; with &quot;1-Wire network&quot;.</td>
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<td></td>
<td>• Rephrased the &quot;benefits of parasite power&quot; statement.</td>
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<tr>
<td></td>
<td>• Replaced references to the Book of iButton Standards with references to corresponding application notes.</td>
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<tr>
<td></td>
<td>• Relocated the $V_{PUP}$ specification from the EC table header to the DC electrical characteristics section.</td>
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<td></td>
<td>• Deleted the $V_{OH}$ parameter from the EC table.</td>
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<td>• In EC table note #2, added a reference to Figure 8.</td>
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